QUANTAR™ TO ASTRO-TAC™ / DIU

CONNECTIONS VIA APRISA XE QUAD V.24 INTERFACE CARD

INTRODUCTION

Motorola's QUANTAR™ base station, ASTRO-TAC™ 3000 comparator, and DIU 3000 products are widely used P25 infrastructure components that use legacy synchronous RS-232/V.24 connections at 9600 bps for transport of Motorola proprietary ASTRO™ voice, data, and signalling information. This method of connection is also supported in the more recent Motorola G-Series site equipment including the GTR 8000 base and GCM 8000 comparator.

The ASTRO protocol used transfers data in a synchronous manner without start/stop bits, unlike normal V.24/RS-232 serial connections. This system is not compatible with standard RS-232 serial linking equipment available today which does not support synchronous operation.

The Aprisa XE QV24S interface card provides four RS-232/V.24 circuits terminated on RJ45 connectors and is programmable for synchronous as well as asynchronous operation. The synchronous mode of this interface is widely used to support Motorola ASTRO V.24 connections.

The ASTRO V.24 interface can be either an actual V.24 physical interface or, in the case of the Quantar, a built-in audio modem that implements a 9600 bps synchronous link over a four wire leased circuit. This note is only for V.24 physical connection applications.

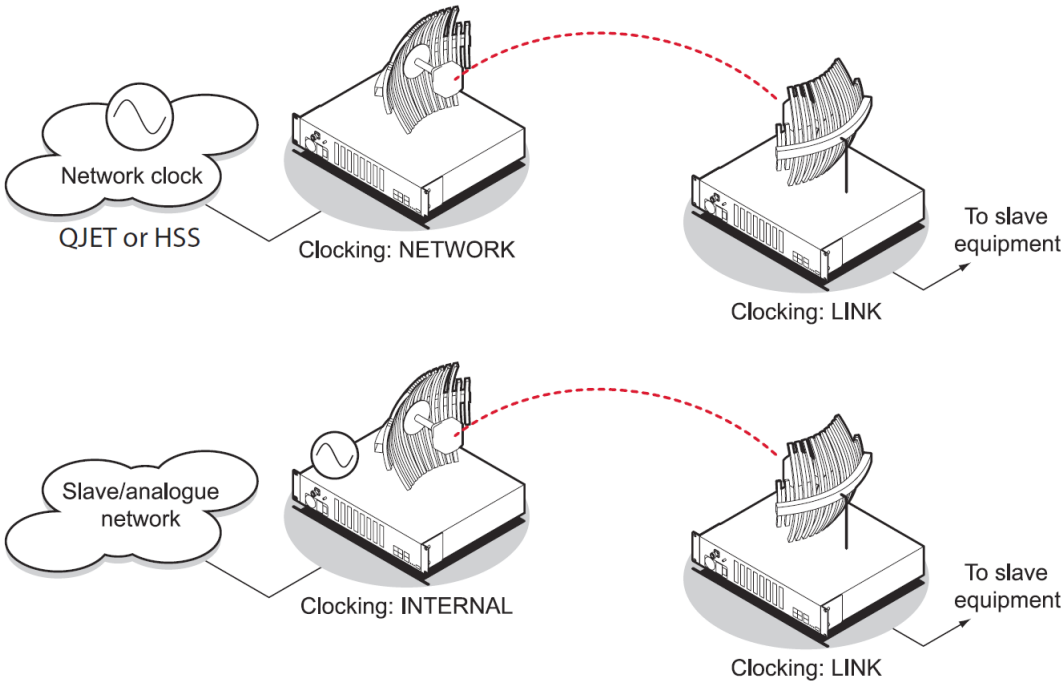
CLOCKING

Clocking integrity is critical in synchronous data networks. In the case of synchronous V.24 networks used for interconnecting Motorola infrastructure components, properly configured clocking will avoid CRC errors and distortion of the digital voice traffic. Satisfactory network clocking can be checked by monitoring the CRC errors at the ASTRO-TAC.

First Step – Terminal Timing

The Aprisa XE links must be configured with appropriately selected terminal clock sources. The diagram below shows two options. If a link is to be established without an E1 or T1 or high-speed network connection, then one end of the link must be set to internal clock, the other end of the link must always be set to link clock. Refer to the Aprisa XE user manual section 'Setting the Terminal Clock Sources'.

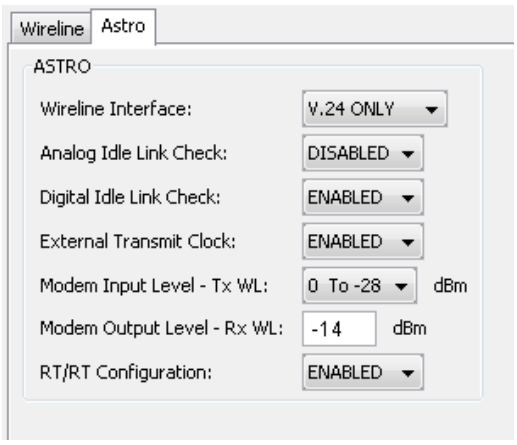
Note that the terminal clocking arrangements are designed to cater for E1/T1 connections via the QJET card or high-speed synchronous connections via the HSS card. The terminal clocking is not related to the clocking used on the low speed V.24 interface. The low speed V.24 clock is independent of the terminal clocking and the card uses a rate adaptation algorithm which allows the V.24 clock to vary by plus or minus 100 parts per million with respect to the terminal timing without error.



Quantar Clocking Options

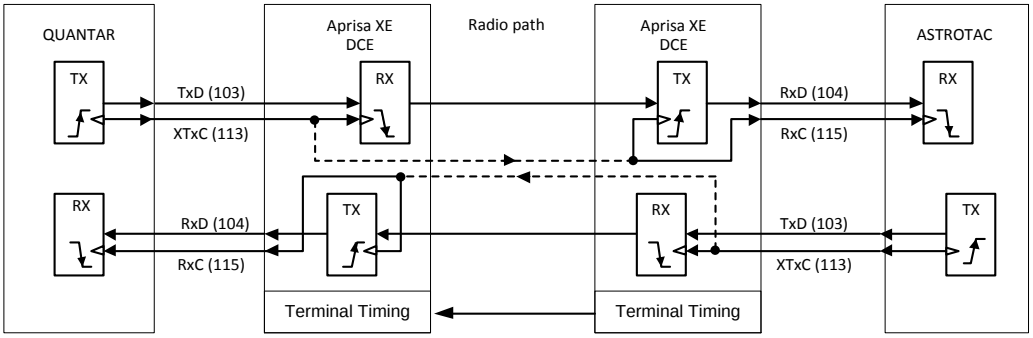
Using the customer service software (CSS) go into the Wireline Config > Astro screens and set the Wireline Interface to the appropriate setting for the application (Hybrid or V.24 Only) and set the External Transmit Clock to disabled. Generally the terminal timing originates from the direction of the core of the network outwards. If the Aprisa is not connected via an E1/T1 circuit to the core then this arrangement is arbitrary, as long as one terminal clock is internal and the other terminal clock is link timed. However, the XE is designed to allow the Quantar clock to flow from the edge to the core independent of the core/telco clock as Motorola generally prefers this arrangement.

An example Quantar CSS Wireline configuration setting is shown below:

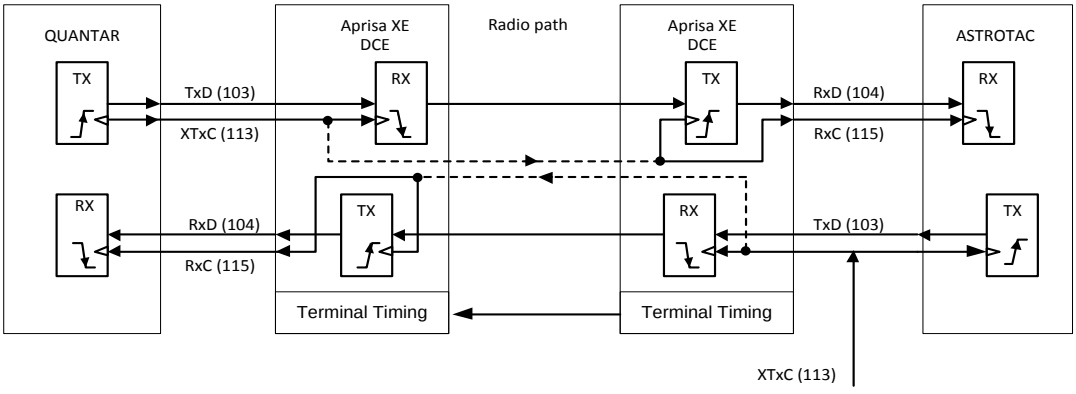


Second Step - Low Speed V.24 Clock

The diagram below shows the basic recommended configuration for connecting the QUANTAR to the ATRO-TAC. For each V.24 signal name there is an associated circuit number shown, as specified in the ITU V.24 data interchange specification. Apart from clock polarity and speed there are no other options for the V.24 low speed synchronous interface. The ATRO-TAC must be programmed to accept input data referenced to an input clock and to output data referenced to clock generated internally within the comparator.



Note that terminal timing originates from the direction of the core of the network outwards. If the Aprisa is not connected via a QJET or HSS interface then this arrangement is arbitrary, as long as one terminal clock is internal and the other terminal clock is link timed.



In the second diagram the ATRO-TAC can operate accepting input data referenced to an input clock and to output data referenced to an external clock, such as would be supplied from a telco network interposed between the Aprisa XE terminal and the ASTRO-TAC. This telco network is not shown in the above diagram to avoid confusion, but the direction and sense of the RxD, RxC, TxD, and XTxC signals must remain as shown. In both cases note that the Quantar clock (recovered from the transmitting subscriber) flows from the edge to the core

The ASTRO-TAC to DIU or QUNATAR to DIU clocking arrangements are similar.

CONNECTIONS

In the case of the Quantar the V.24 physical interface is implemented by means of a Motorola supplied TTN4010 V.24 daughter card. In the case of the ASTRO-TAC and DIU equipment these devices have V.24 physical interfaces as standard. The Aprisa XE to Quantar connections are as follows:

RJ45 quad V.24 card on Aprisa XE

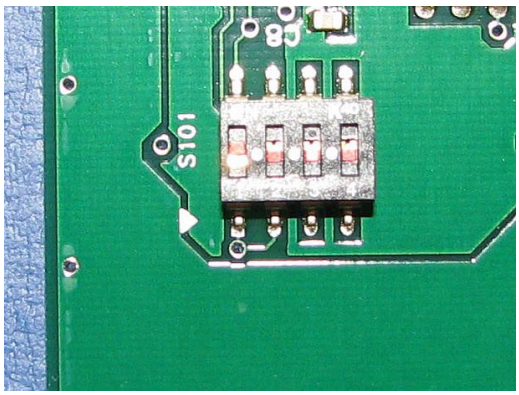
1	RTS from Quantar
2	TX clock from Quantar
3	TX data from Quantar
4	GND
5	GND
6	RX data to Quantar
7	RX clock to Quantar
8	CTS to Quantar

There are two LED status indicators on each of the Aprisa XE RJ45 connectors. The yellow LED flashes to show activity on the RX while the green LED show activity on the TX. Further technical details on the XE are in the user manual in the section 'Interface Connections'.

RJ45 on Quantar

1	RX clock to Quantar
2	CD input to Quantar
3	TX clock from Quantar
4	GND
5	RX data to Quantar
6	TX data from Quantar
7	CTS to Quantar
8	RTS from Quantar

The RJ45 is located on the front of the Quantar SCM and is the lower of the two RJ45 ports. It may be necessary to check the switch settings on the Quantar V.24 daughter board located on the Wireline card. The settings should be as follows:

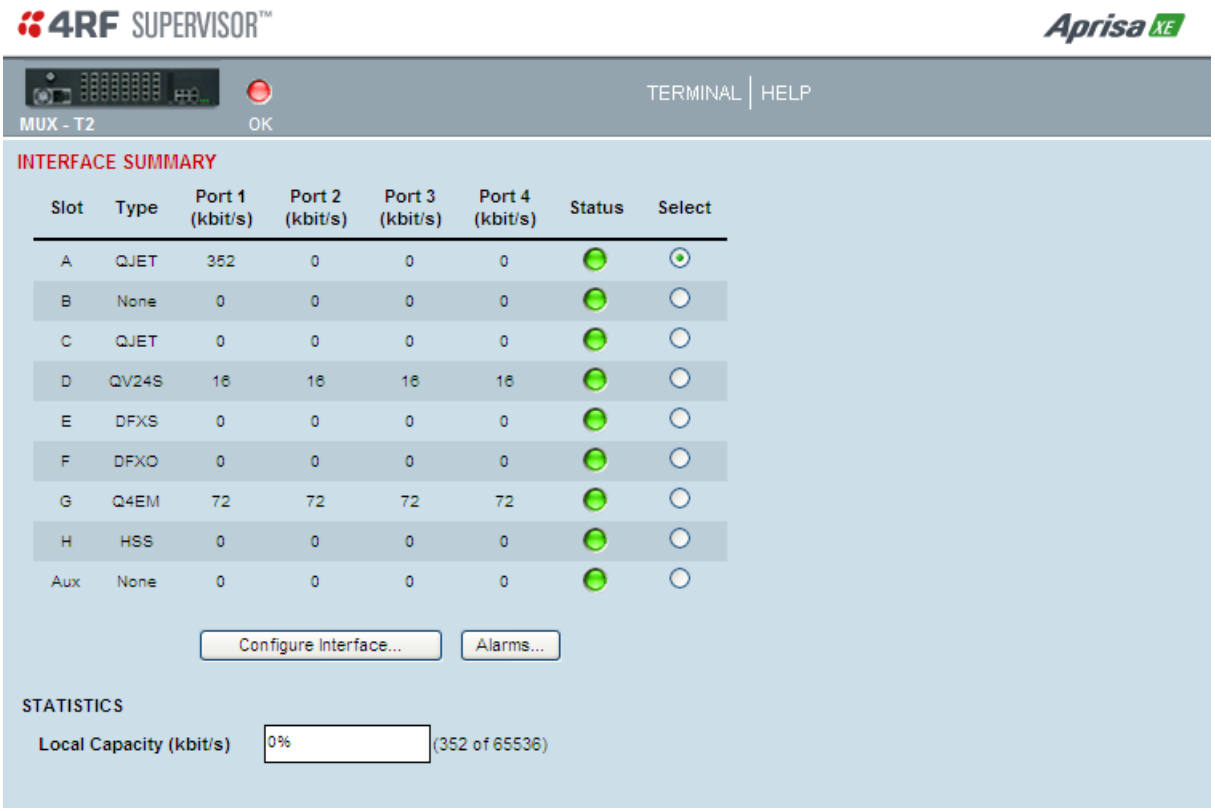


Switch 1 of S101 should be on and the other switches off. S1 off sets CTS off rather than feeding through CTS from the external interface while S2 on loops RTS to CTS.

APRISA SUPERVISOR SETTINGS

It is necessary to set the Aprisa XE quad V.24 card for synchronous operation using the web set up SUPERVISOR tool.

Open SUPERVISOR, in the menu open Interface > Slot Summary, from the list select the slot to editing (radio button on the right 'Select'), press button <Configure slot..>, it will open next page 'Edit Interface Slot', set appropriate interface card in the 'Expected' menu and the same in 'Change Type To' menu and press <Apply> button. It should be QV24S as shown in slot D of this SUPERVISOR settings screen shot:



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